

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,623,997	November 18, 1986	Tulpule			
	5,627,992	May 6, 1997	Baror			
	5,696,791	December 9, 1997	Yeung			
	5,804,986	September 8, 1998	Jones			
	6,049,866	April 11, 2000	Earl			
	6,553,479	April 22, 2003	Mirsky et al.			
	6,598,128	July 22, 2003	Yoshioka et al.			
	6,745,317	June 1, 2004	Mirsky et al.			
	6,751,722	June 15, 2004	Mirsky et al.			
	7,028,107	April 11, 2006	Vorbach et al.			
	7,595,659	September 29, 2009	Vorbach et al.			
	7,650,448	January 19, 2010	Vorbach et al.			
	2001/0003834	June 14, 2001	Shimonishi			
	2002/0156962	October 24, 2002	Chopra et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	2001-167066	June 22, 2001	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	
	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.	
	IMEC, "ADRES multimedia processor & 3MF multimedia platform," Transferable IP, IMEC Technology Description, (Applicants believe the date to be October 2005), 3 pages.	
	Kanter, David, "NVIDIA's GT200: Inside a Parallel Processor," <a href="http://www.realworldtech.com/page.cfm?ArticleID=RW090989195242&amp;p=1">http://www.realworldtech.com/page.cfm?ArticleID=RW090989195242&amp;p=1</a> , September 8, 2008, 27 pages.	
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," (v2.2) September 10, 2002, Xilinx Production Product Specification, pp. 1-52.	
	XILINX, "Virtex-II and Virtex-II Pro X FPGA Platform FPGAs: Complete Data Sheet," (v4.6) March 5, 2007, pp. 1-302.	
	XILINX, "Virtex-II Platform FPGAs: Complete Data Sheet," (v3.5) November 5, 2007, pp. 1-226.	
EXAMINER	/Idriss Alrobaye/	DATE CONSIDERED 07/07/2010
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		